☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: V500HK1
SUFFIX: PS5

Customer:
CONFIRMED BY **SIGNATURE**

Name / Title _____ _____

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	WT Hsu

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	8,Mar 2012 19,Jun 2012	All 36	All 10	The Approval specification was first issued. Update MECHANICAL DRAWING

1. GENERAL DESCRIPTION

1.1 OVERVIEW

35-D076901 is a control board for V500HK1-PS5 model.

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Interface	2ch LVDS.
White tracking function	Support white tracking function.
Over drive	Support over drive function.
Color Depth	8 bit

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

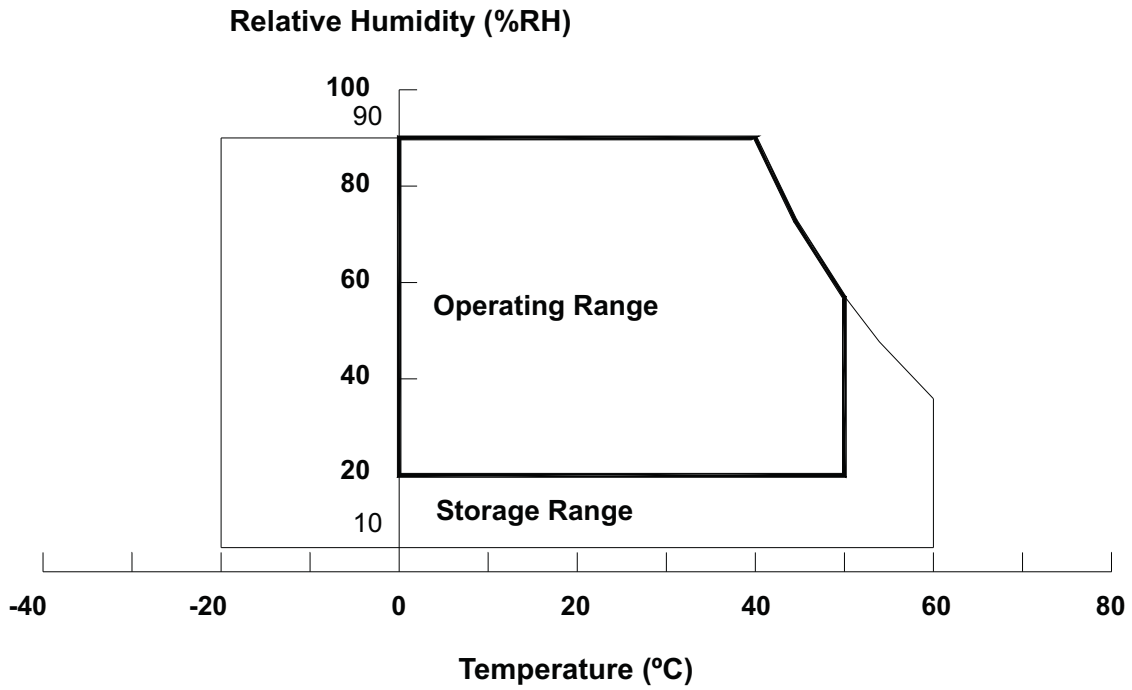
Item	ymbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	$_{ST}$	-20	+60	C	(1), (3)
Operating Ambient Temperature	$_{OP}$	0	50	C	(1), (2), (3)
Altitude Operating	$_{OP}$	0	5000		(3)
Altitude Storage	$_{ST}$	0	12000		(3)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation..



Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.2 PACKAGE STORAGE

Storage condition: With shipping package.

Storage temperature rang: 25±5℃

Storage humidity range: 50±10%RH

Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

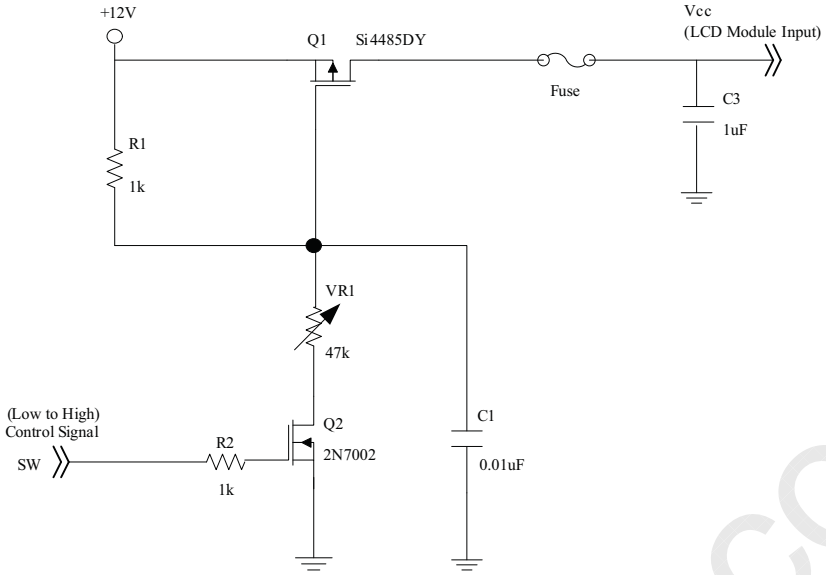
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

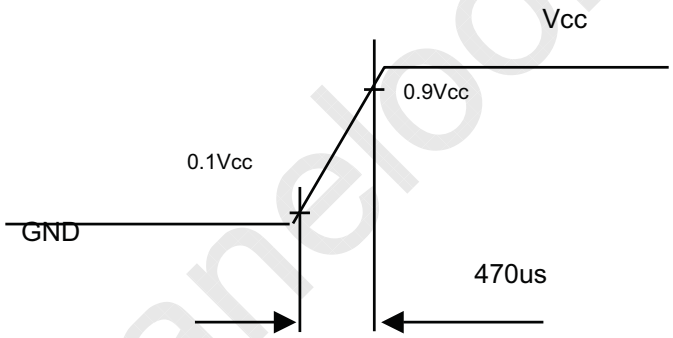
Parameter			Symbol	Value			Unit	Note
				Min.	Typ.	Max.		
Power Supply Voltage			V_{CC}	10.8	12	13.2	V	(1)
Rush Current			I_{RUSH}	–	–	3.06	A	(2)
Power Consumption		White Pattern	–	–	6.6	7.1	W	(3)
		Horizontal Stripe	–	–	14	18.1	W	
		Black Pattern	–	–	6.5	7.0	W	
Power Supply Current		White Pattern	–	–	0.55	0.60	A	
		Horizontal Stripe	–	–	1.2	1.5	A	
		Black Pattern	–	–	0.54	0.59	A	
LVDS interface	Differential Input High Threshold Voltage		V_{LVTH}	+100	–	–	mV	(4)
	Differential Input Low Threshold Voltage		V_{LVTL}	–	–	-100	mV	
	Common Input Voltage		V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)		$\|V_{ID}\|$	200	–	600	mV	
	Terminating Resistor		R_T	–	100	–	ohm	
CMIS interface	Input High Threshold Voltage		V_{IH}	2.7	–	3.3	V	
	Input Low Threshold Voltage		V_{IL}	0	–	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

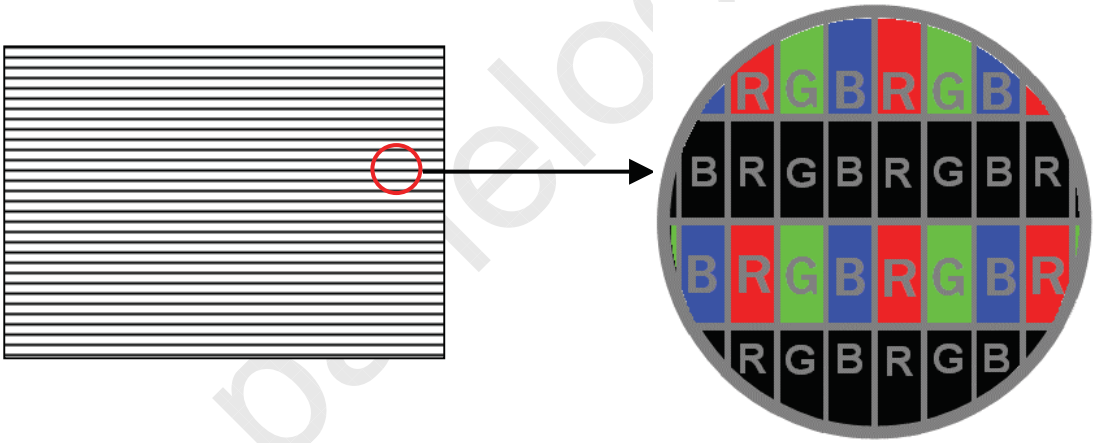
a. White Pattern

Active Area

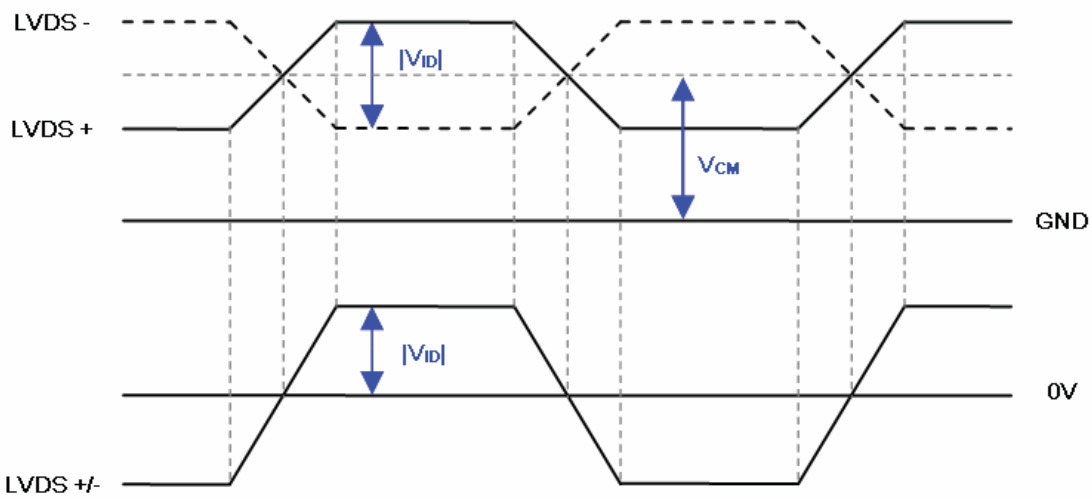
b. Black Pattern

Active Area

c. Horizontal Pattern

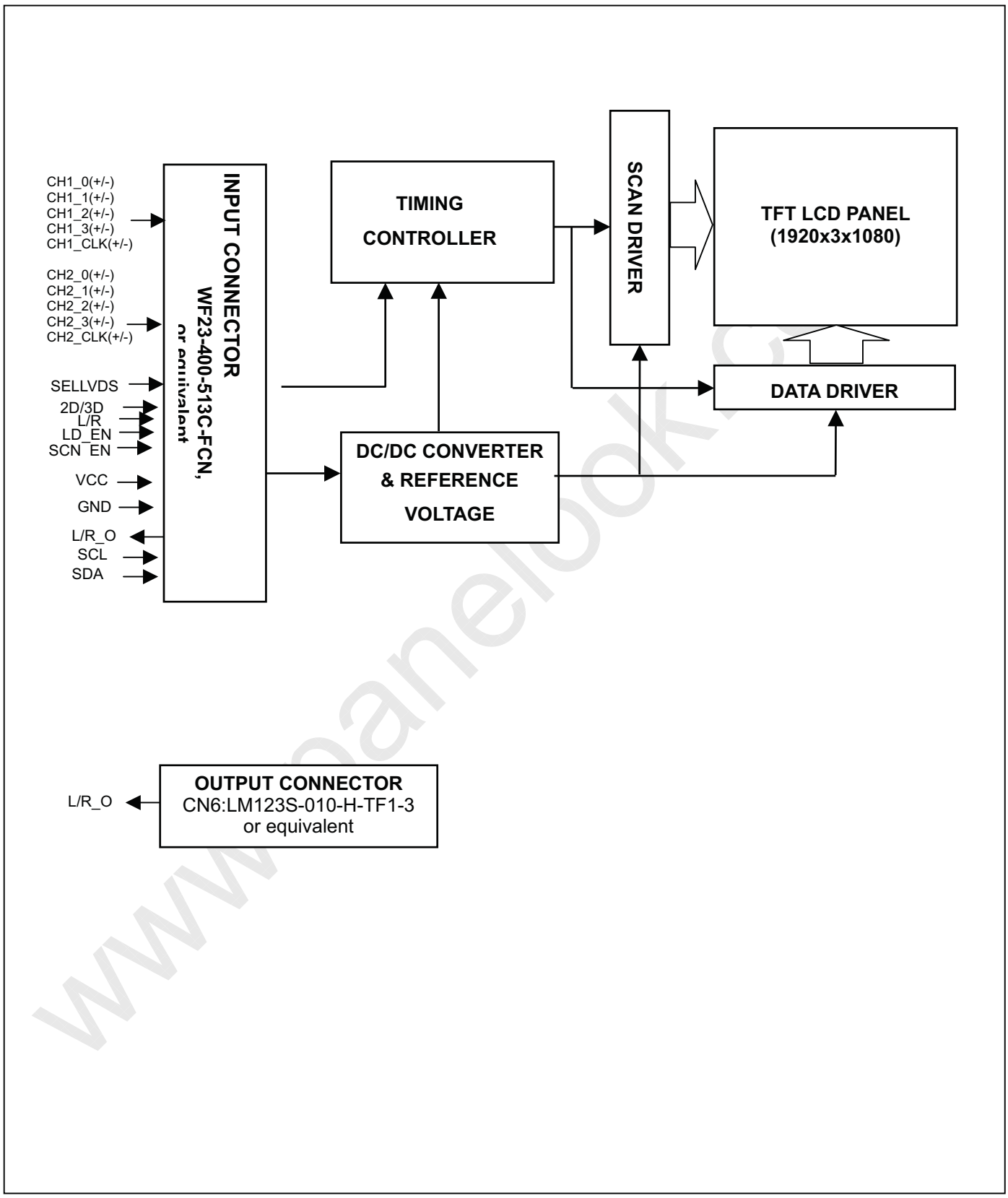


Note (4) The LVDS input characteristics are as follows :



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD OPEN CELL

CNF1 Connector Pin Assignment: (WF23-400-513C-FCN or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	SCL	I2C Serial Clock (for 3D format selection function)	(11)
3	SDA	I2C Serial Data (for 3D format selection function)	
4	AGMODE	Aging Mode	(12)
5	L/R_O	Output signal for Left Right Glasses control	(10)
6	N.C.	No Connection	(1)
7	SELLVDS	Input signal for LVDS Data Format Selection	(2)(7)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(9)
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input	(9)
20	OCLK+	Odd pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(9)
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(6)(8)
27	L/R	Input signal for Left Right eye frame synchronous(Frame sequence mode)	(4)(8)
28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(9)
29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	

30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input.	(9)
36	ECLK+	Even pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(9)
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	
42	LD_EN	Input signal for Local Dimming Enable	(5)(8)
43	SCN_EN	Input signal for Scanning Enable	(6)(8)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CN1 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(10)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or open

SELLVDS	Note
L	JEIDA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Input signal for Left Right eye frame synchronous

V_{IL}=0~0.8 V, V_{IH}=2.0~3.3 V

L/R	Note
L	Right synchronous signal
H	Left synchronous signal

Note (5) Local dimming enable selection.

L= Connect to GND, H=Connect to +3.3V or Open

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

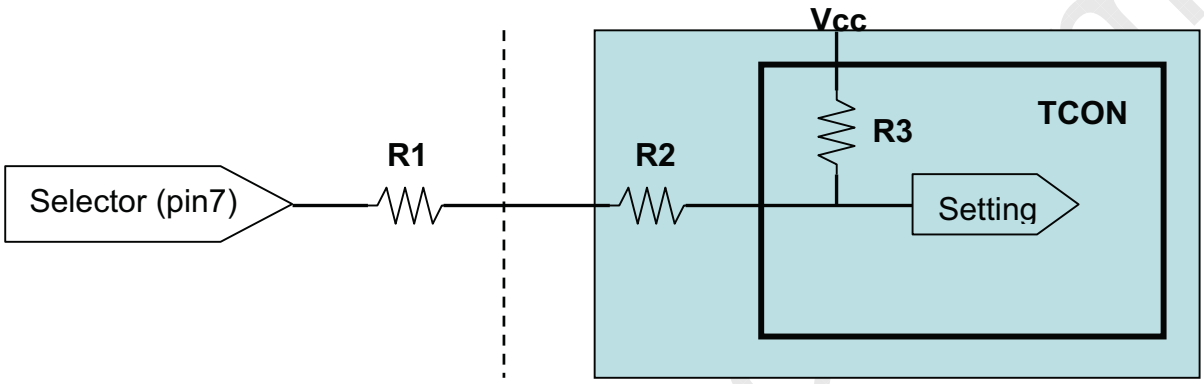
Note (6) Scanning enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

SCN_EN	Note
L or Open	Scanning Disable
H	Scanning Enable

Note (7) SELLVDS, LD_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)

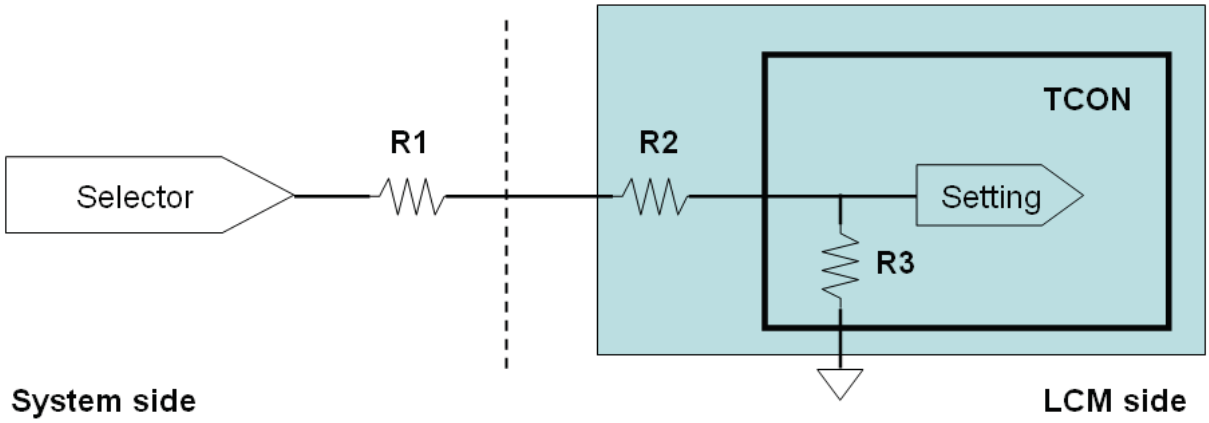


System side

R1 < 1K

Note (8) 2D/3D, L/R and SCN_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



System side: R1 < 1K

Note (9) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

Note (10) The definition of L/R_O signal as follows

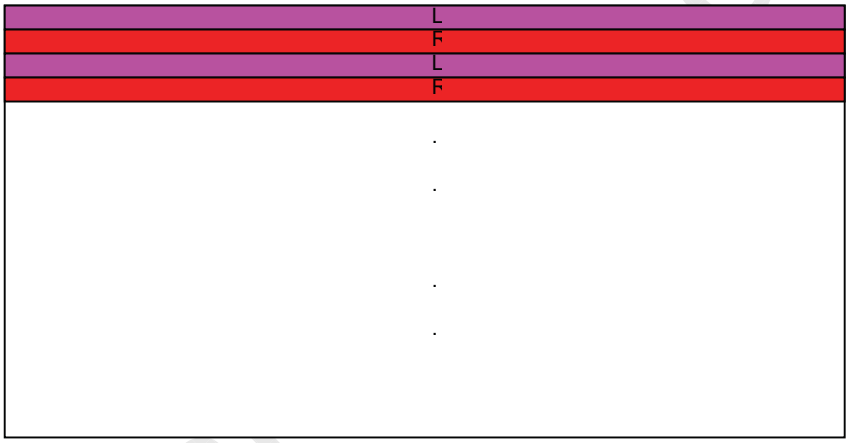
L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

Note (11) Please reference Appendix A

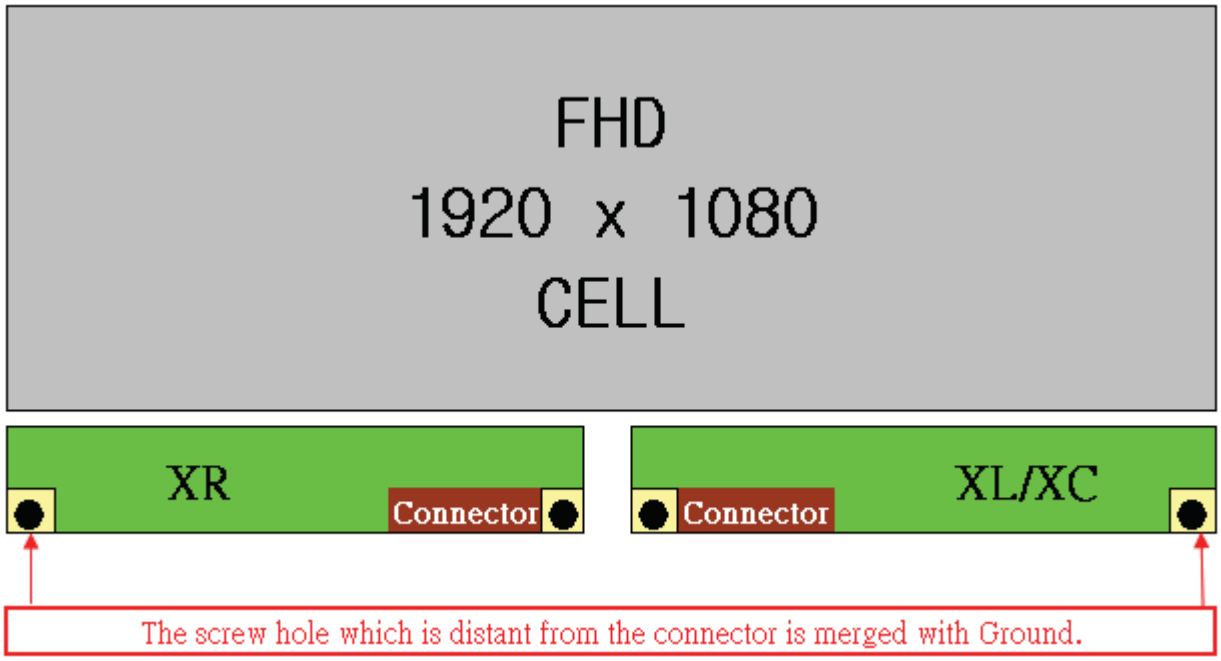
Note (12) Ground or OPEN: Disable, High: Enable.

Note (13)Currently, we only support line alternative format (1st line is left signal), show as the attached block diagram. In the future, we will support other format.

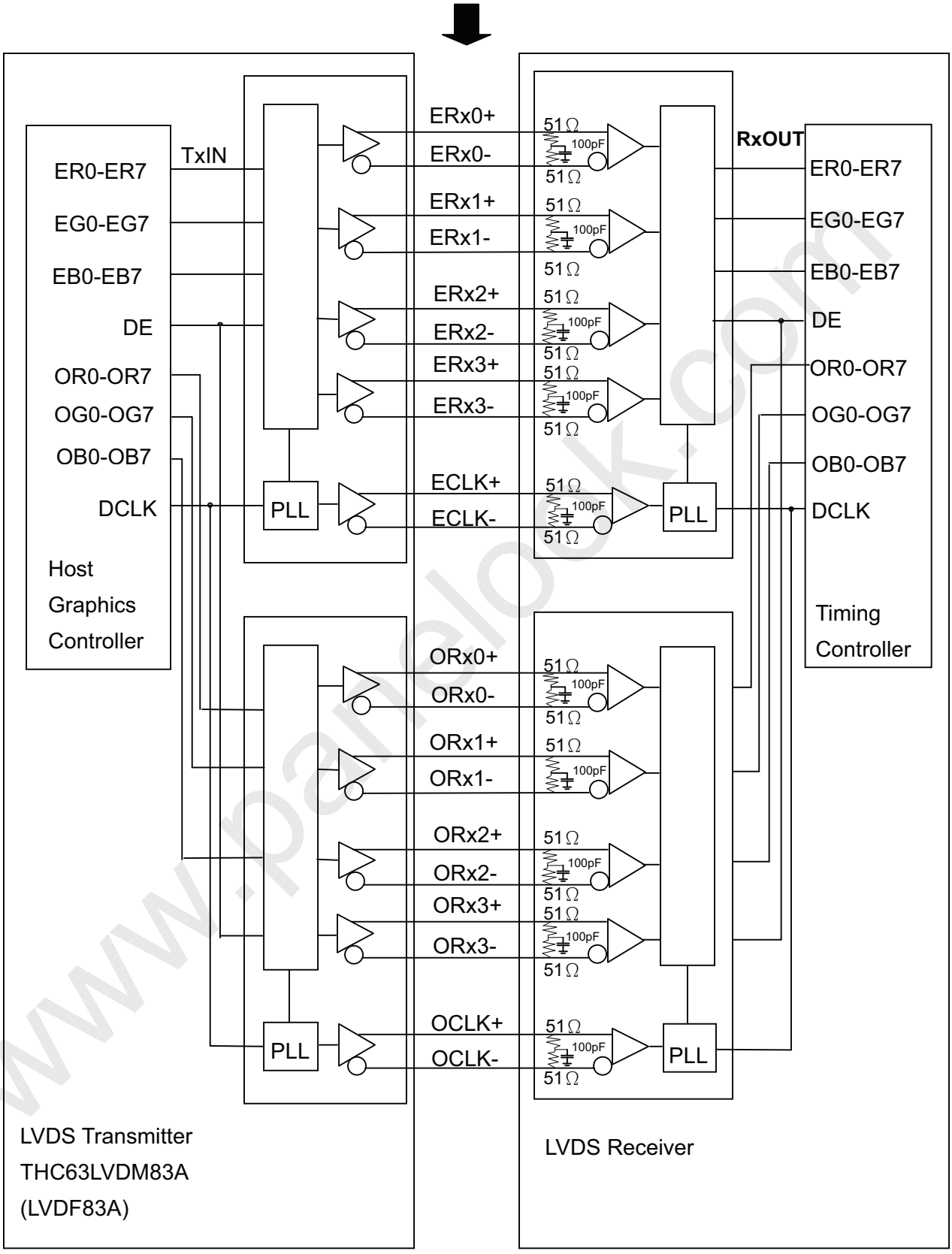


Line alternative format

Note (14) The screw hole which is distant from the connector is merged with Ground



BLOCK DIAGRAM OF INTERFACE



ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

DE: Data enable signal

DCLK: Data clock signal

Note (1) The system must have the transmitter to drive the module.

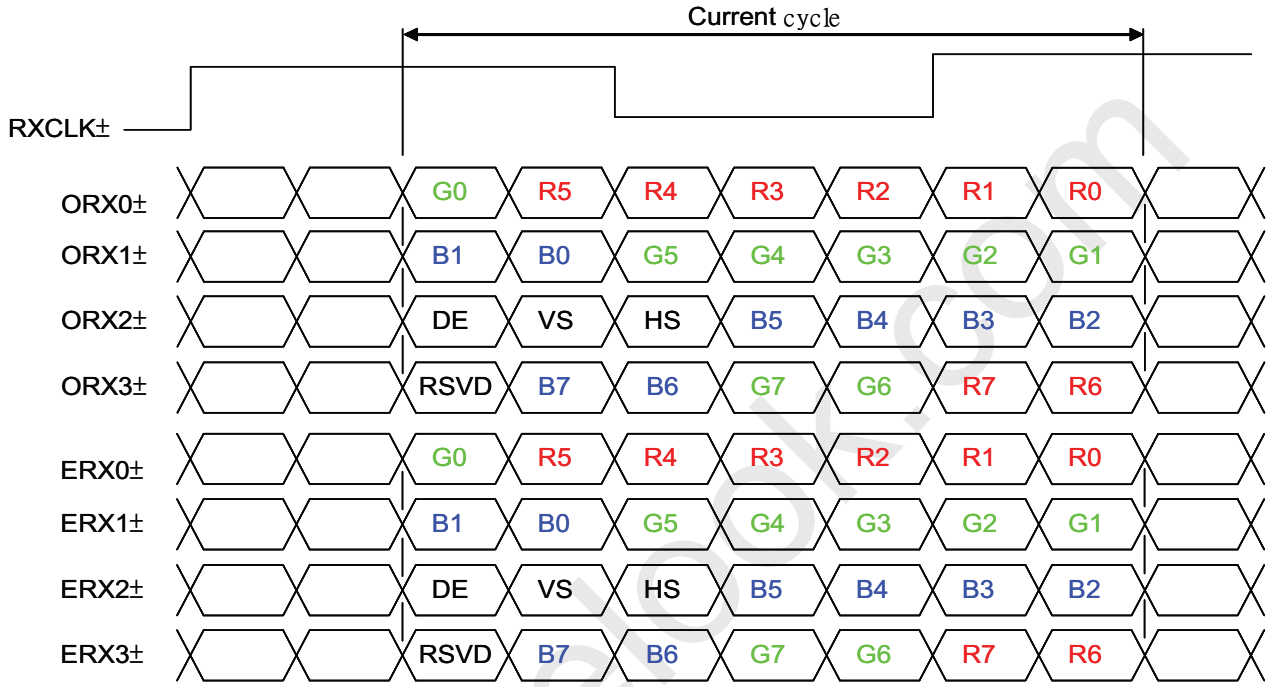
Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.2 LVDS INTERFACE

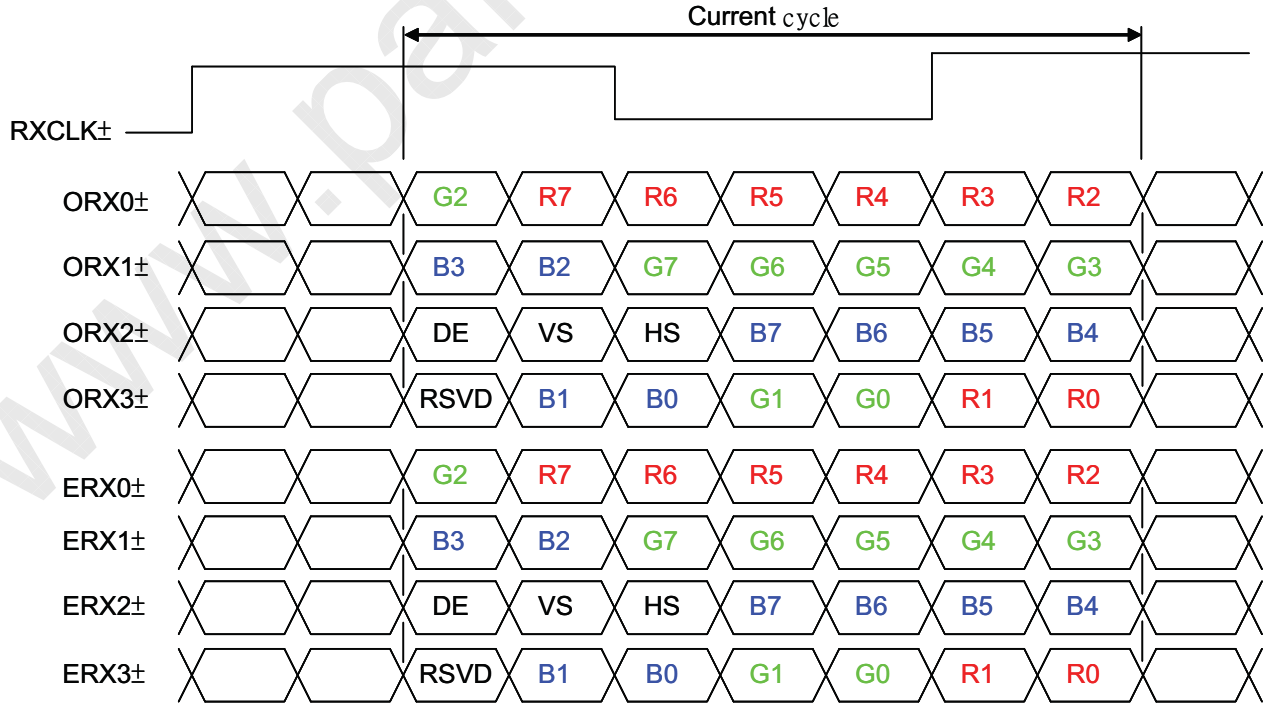
JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

VESA LVDS format



JEDIA LVDS format



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

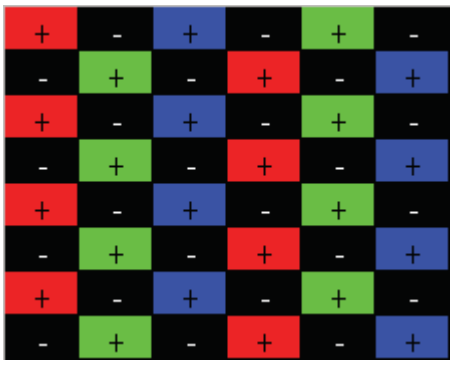
Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.4 FLICKER (Vcom) ADJUSTMENT

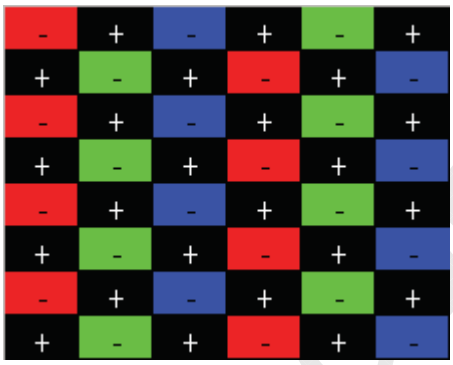
(1) Adjustment Pattern:

Column-inversion pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.

Frame N



Frame N+1



(2) Adjustment method: (Auto-Gamma)

Programmable memory IC is used for Auto-Gamma adjustment in this model. CMI provide Auto Vcom tools to adjust Auto-Gamma.The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto-Gamma adjustment OI. Below items is suggested to be ready before Auto-Gamma adjustment in customer LCM line.

a. USB Sensor Board.

b. Programmable software

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	77	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(2)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(3)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	-	400	ps	(4)

6.1.1 Timing spec for Frame Rate = 50Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	47	50	53	Hz	
	3D mode		F_{r5}	50	50	50	Hz	(6)
Vertical Active Display Term	2D Mode	Total	Tv	1115	1125	1380	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	35	45	300	Th	—
	3D Mdoe	Total	Tv	1350			Th	(5), (7)
		Display	Tvd	1080			Th	
		Blank	Tvb	270			Th	
Horizontal Active Display Term	2D Mode	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
		Display	Thd	960	960	960	Tc	—
		Blank	Thb	90	140	190	Tc	—
	3D Mdoe	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
		Display	Thd	960	960	960	Tc	—
		Blank	Thb	90	140	190	Tc	—

6.1.2 Timing spec for Frame Rate = 60Hz

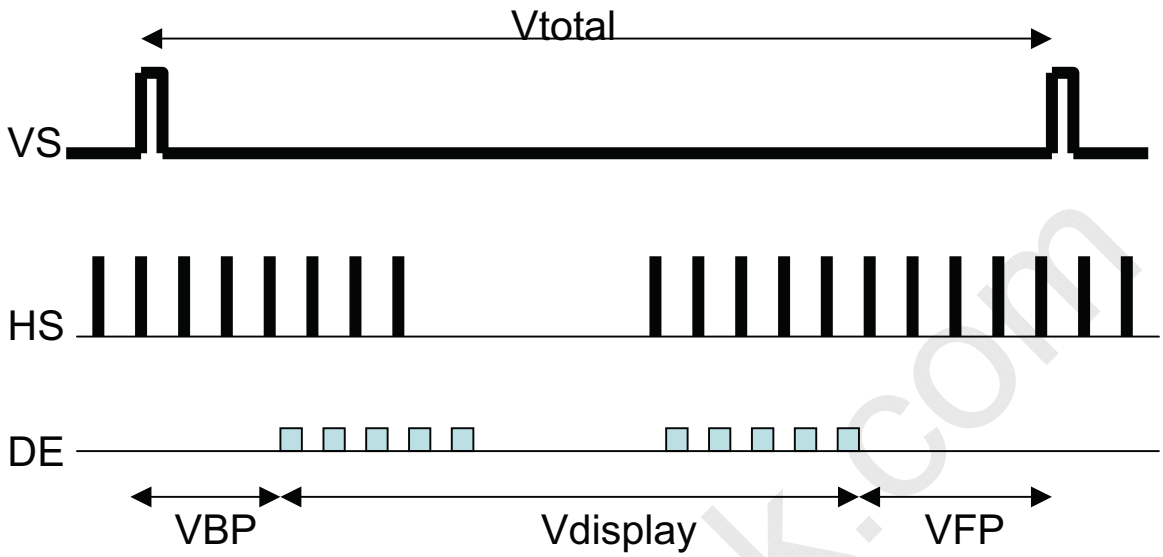
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	57	60	62.5	Hz	
	3D mode		F_{r6}	60	60	60	Hz	(6)
Vertical Active Display Term	2D Mode	Total	Tv	1115	1125	1380	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	35	45	300	Th	—
	3D Mdoe	Total	Tv	1125			Th	(5), (7)
		Display	Tvd	1080			Th	
		Blank	Tvb	45			Th	
Horizontal Active Display Term	2D Mode	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
		Display	Thd	960	960	960	Tc	—
		Blank	Thb	90	140	190	Tc	—
	3D Mdoe	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
		Display	Thd	960	960	960	Tc	—
		Blank	Thb	90	140	190	Tc	—

Note(1) Please make sure the range of pixel clock has follow the below equation:

$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

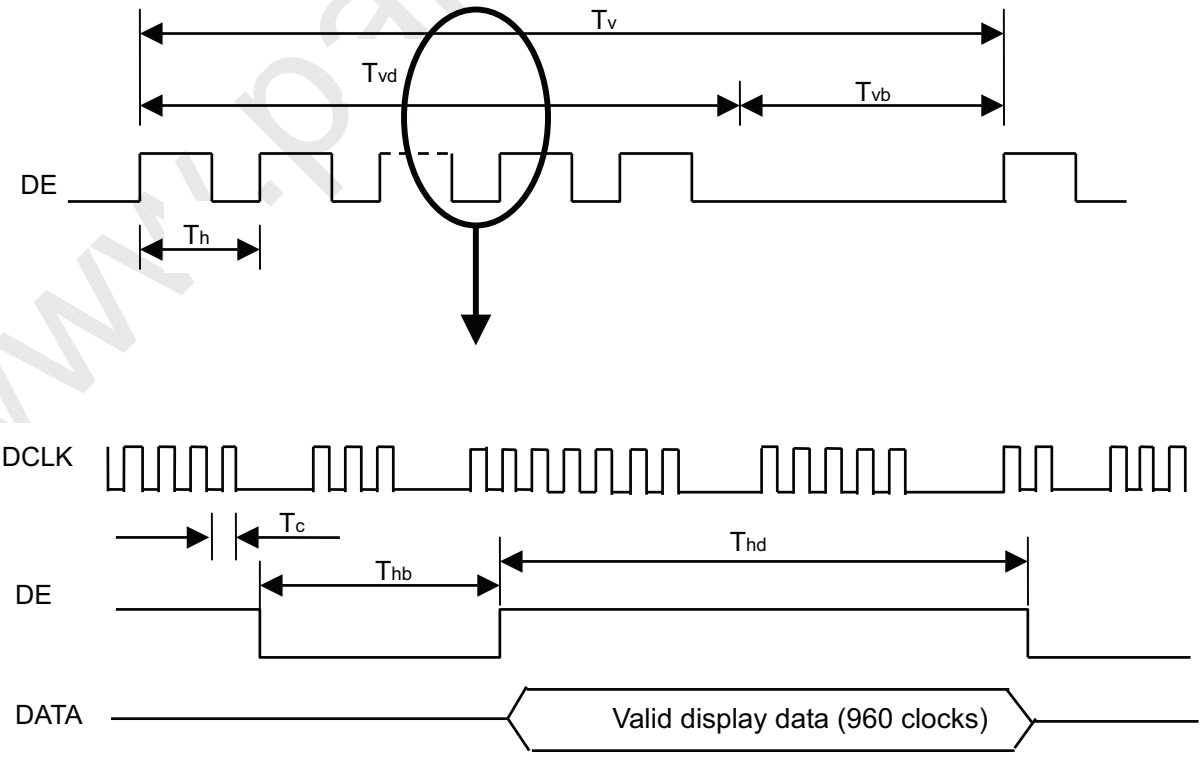
$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

INPUT SIGNAL TIMING DIAGRAM

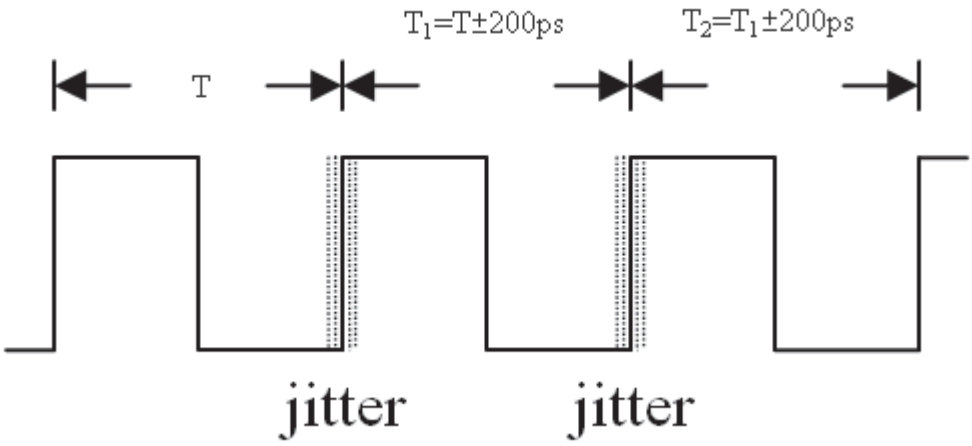


- VBP max : 150 line

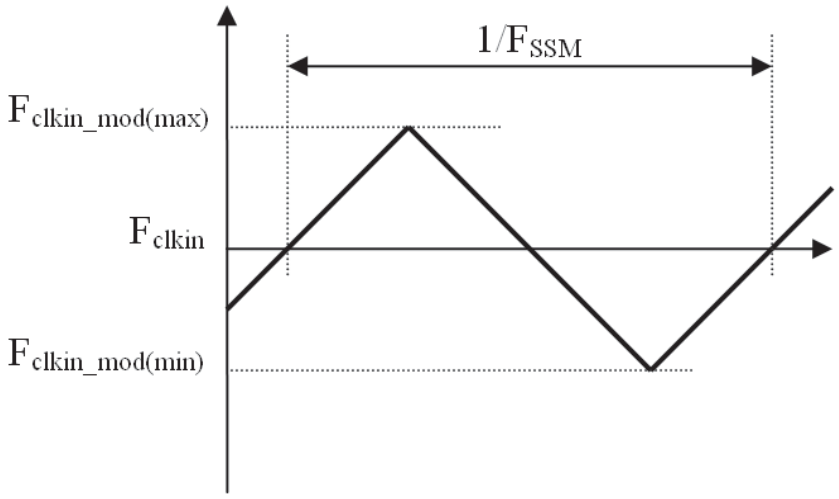
  Suggest VBP = VFP = ½ * (Vtotal - Vdisplay)



Note (2) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

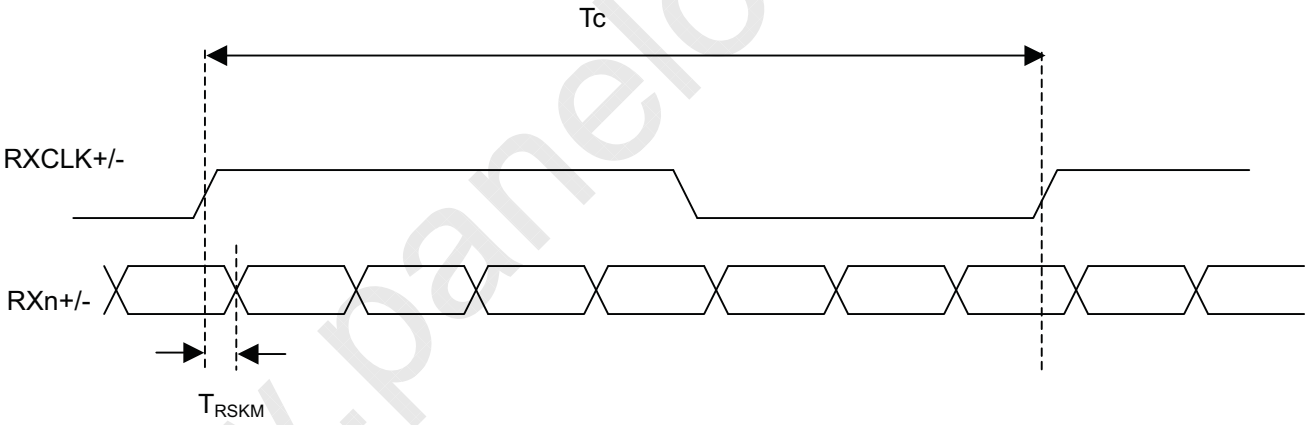


Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (4) LVDS receiver skew margin is defined and shown as below.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (5) Please fix the Vertical timing (Vertical Total =1350 / Display =1080 / Blank = 270) in 50Hz 3D mode and Vertical timing (Vertical Total =1125 / Display =1080 / Blank = 45) in 60Hz 3D mode

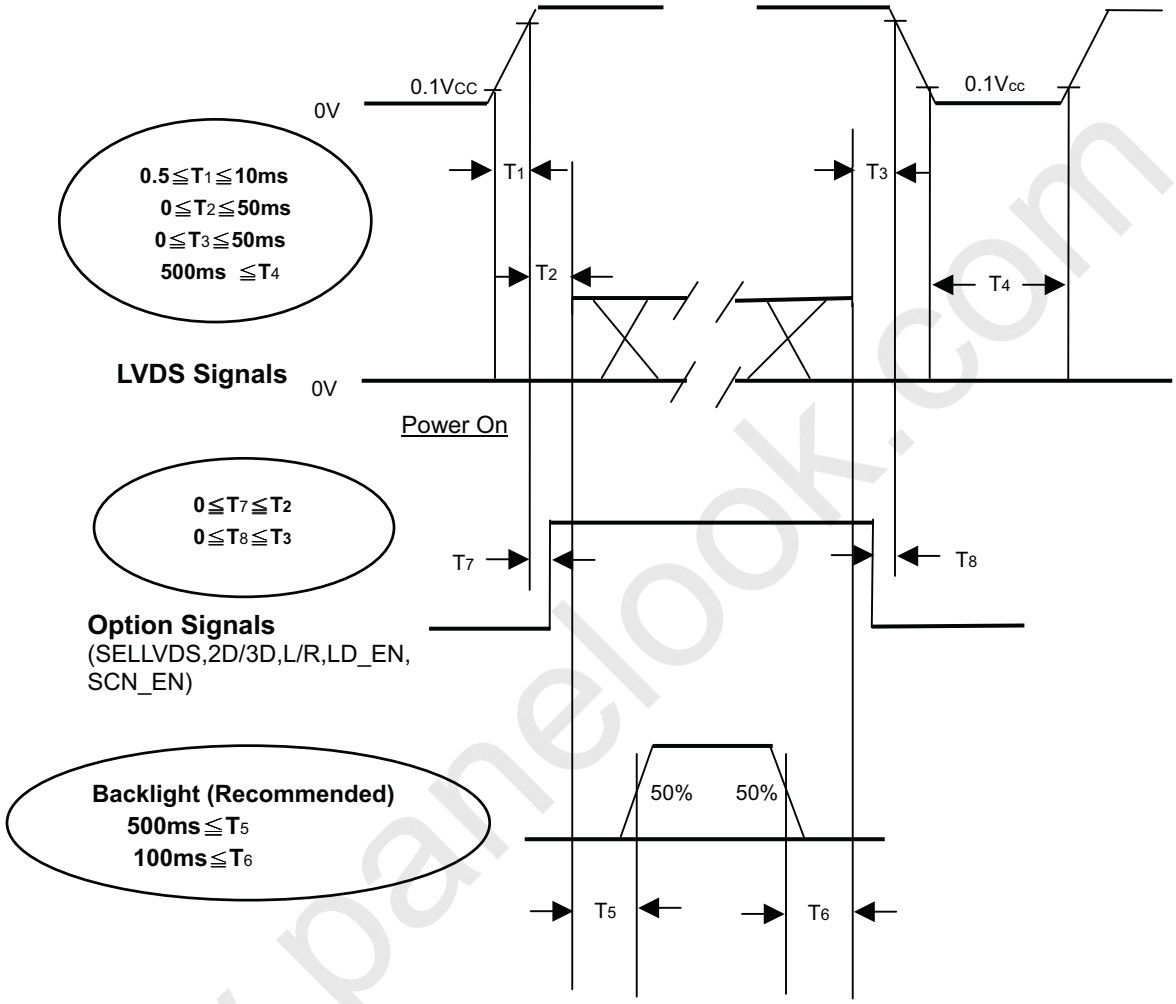
Note (6) In 3D mode, the set up Fr5 and Fr6 in Typ. ±3 Hz .In order to ensure that the electric function performanceto avoid no display symptom.(Except picture quality symptom.)

Note (7) In 3D mode, the set up Tv and Tvb in Typ. ±30.In order to ensure that the electric function performance toavoid no display symptom.(Except picture quality symptom.)

6.2 POWER ON/OFF SEQUENCE (Ta = 25 ± 2 ºC)

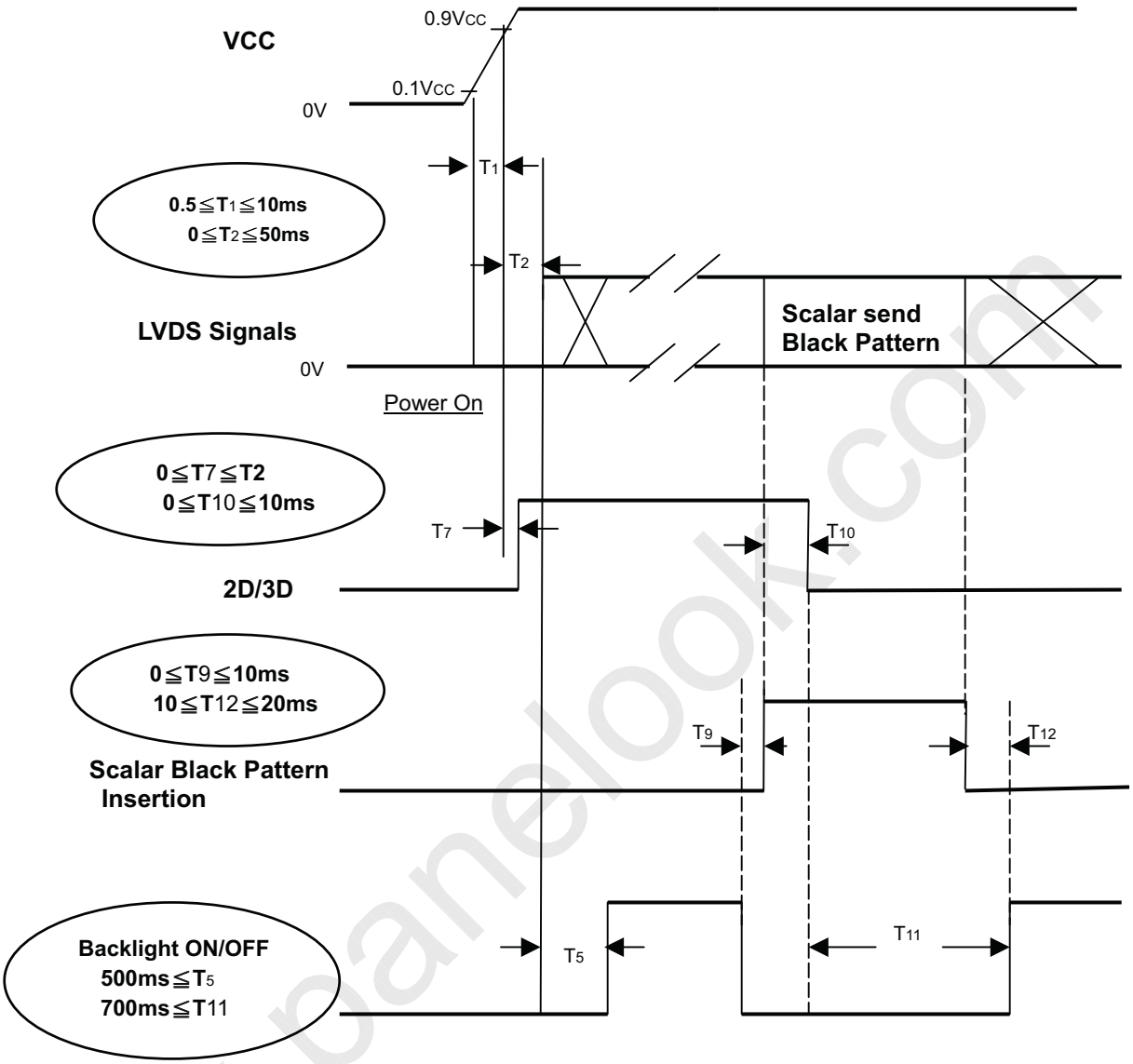
6.2.1 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

6.2.2 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) When 2D/3D mode is changed, TCON will insert black pattern internally. During black insertion, TCON would load required optical table and TCON parameter setting. The black insertion time should be longer than 650ms because TCON must recognize 2D or 3D format and set the correct parameter.

Note (7) 2D/3D switching time should be larger than 500ms

7. PRECAUTIONS

7.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

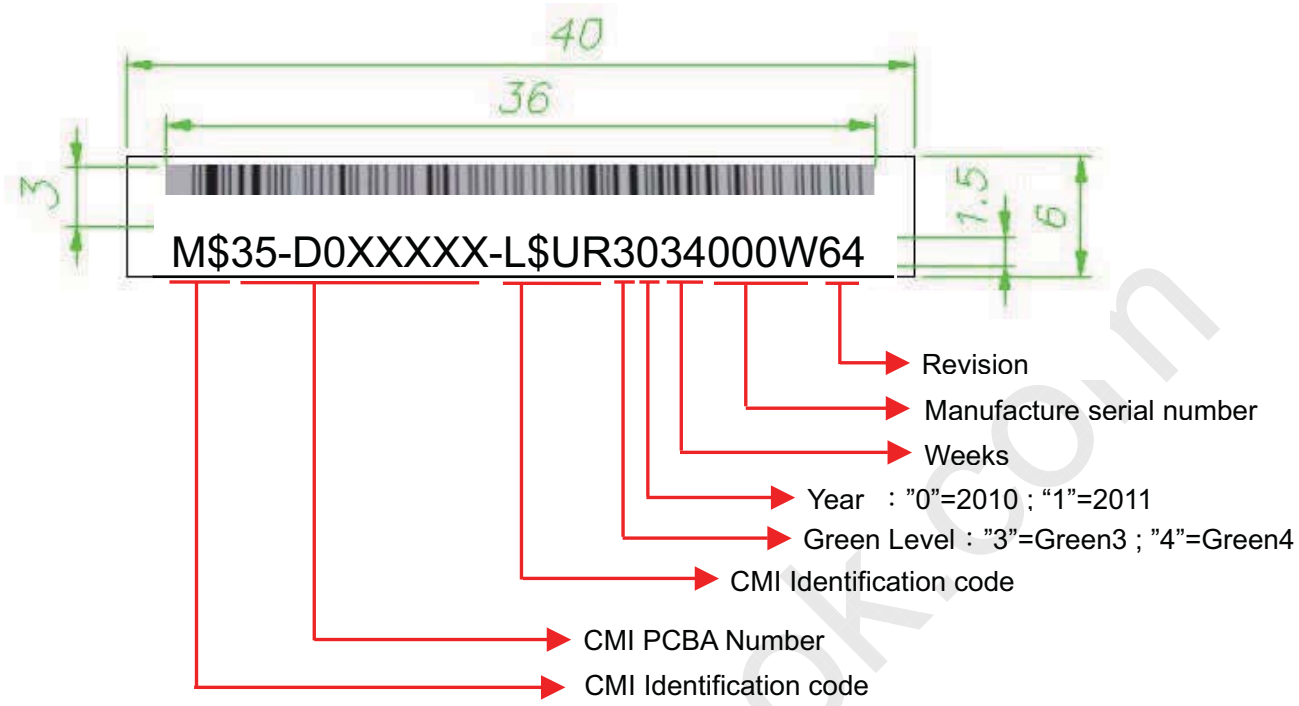
[3] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[4] Do not plug in or pull out the I/F connector while the module is in operation.

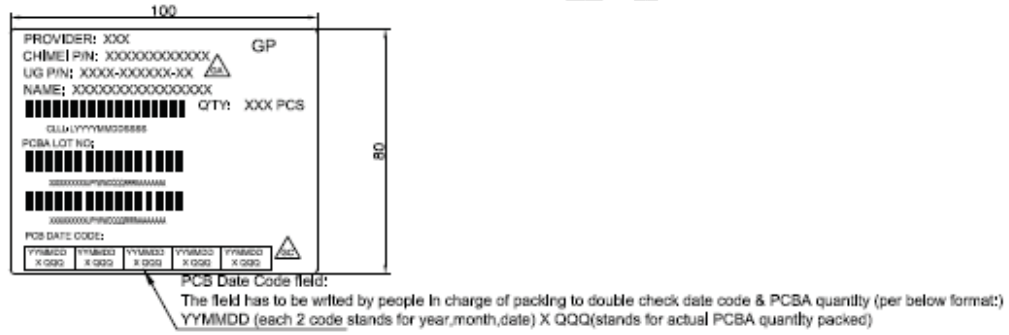
[5] When storing Tcon boards as spares for a long time, the following precaution is necessary.
Do not leave the Tcon boards in high temperature, and high humidity for a long time. It is highly recommended to store the Tcon boards with temperature from 0 to 35℃at normal humidity without condensation.

8. DEFINITION OF LABELS

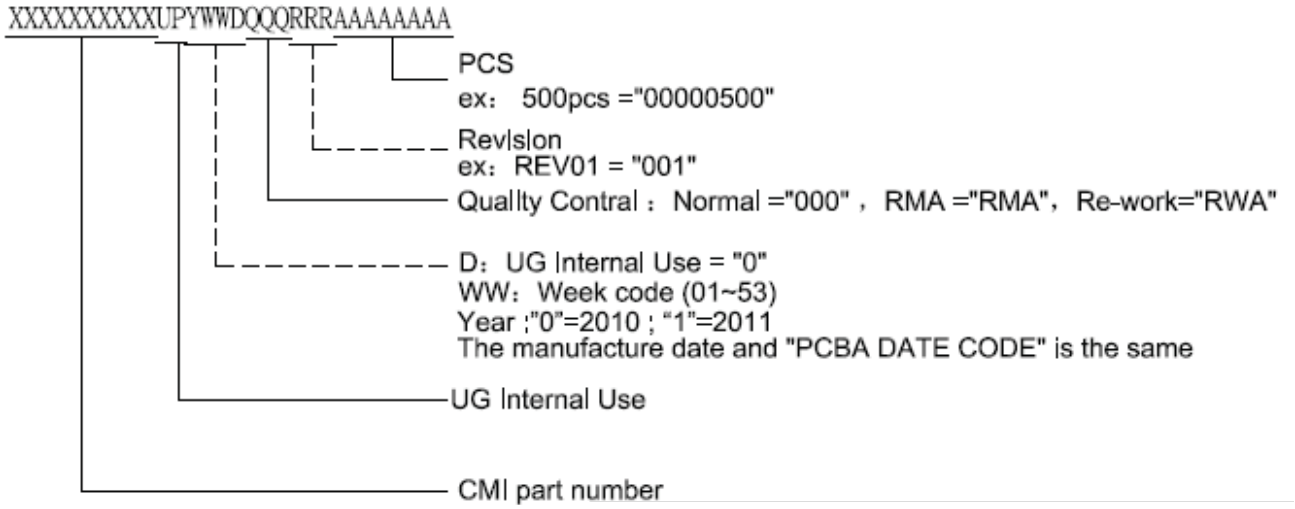
8.1 Label of Tcon



8.2 Label of Tcon package



1. PCBA LOT NO:



9. PACKAGING ：

9.1 PACKAGING SPECIFICATIONS

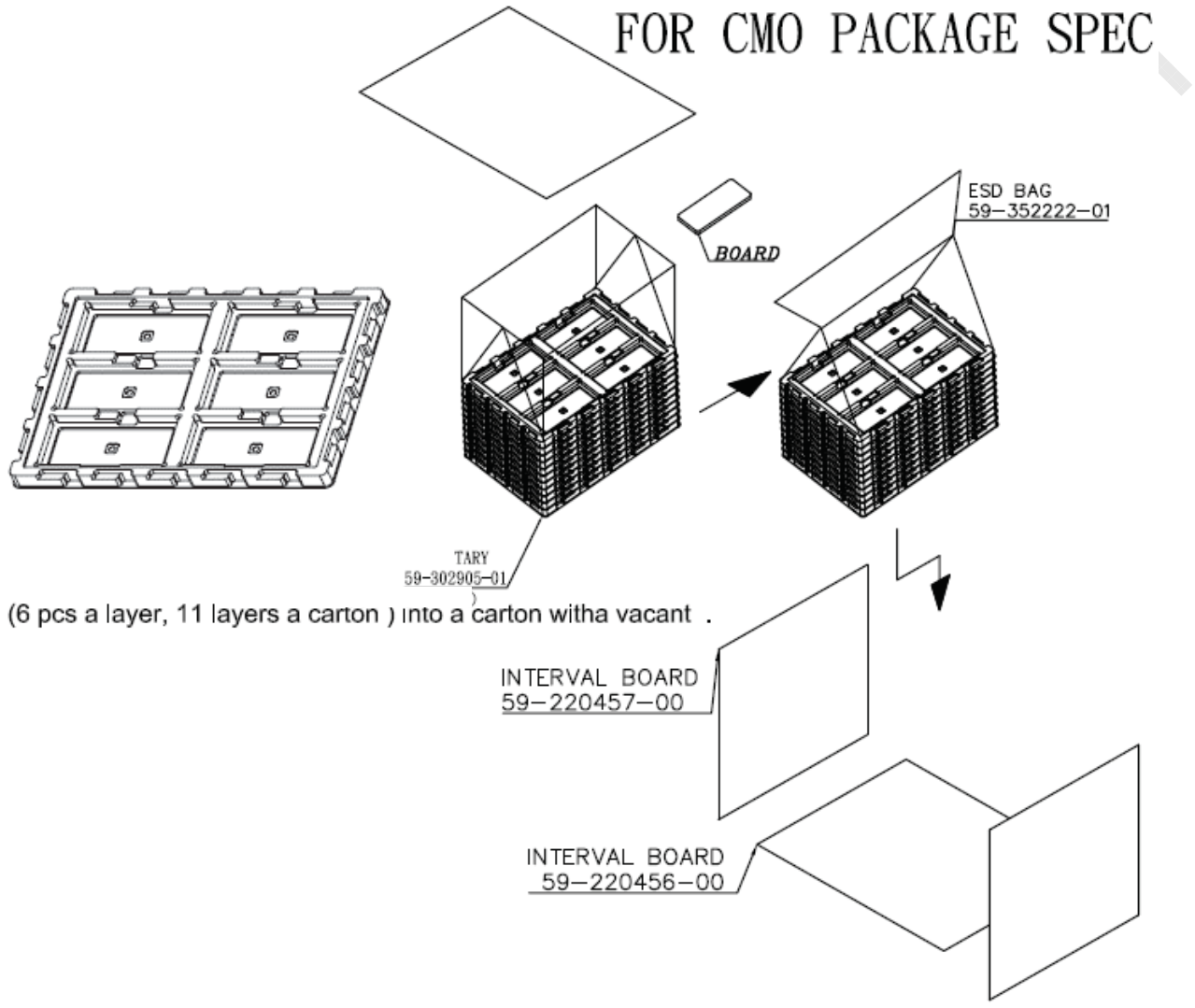
(1) UG 10 Layer , 60 pcs / 1 Box ；TSMT 22 Layer , 132 pcs / 1 Box

(2) Box dimensions : UG 445(L)x320(W)x206(H)mm ；TSMT 467(L)x338(W)x306(H)mm

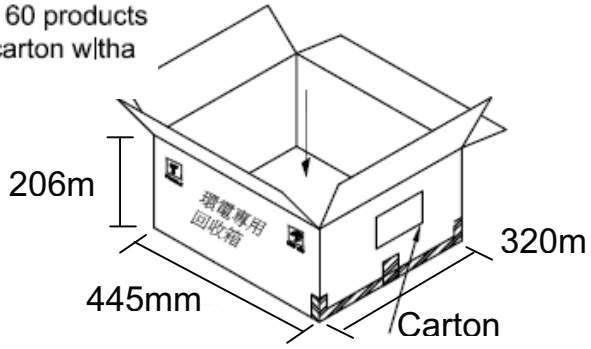
(3) Weight : Approx. UG 5.2Kg (1 Box) ；TSMT 10.5Kg (1 Box)

9.2 PACKAGING METHOD

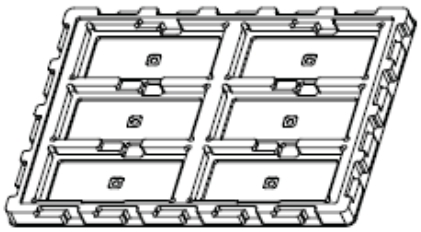
UG

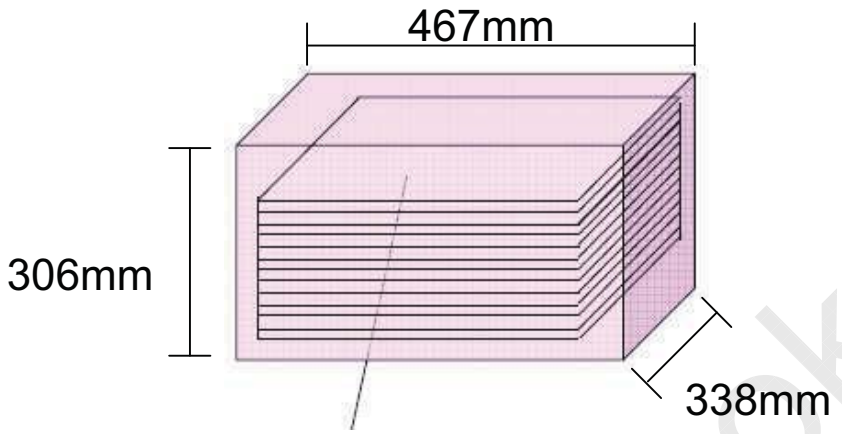


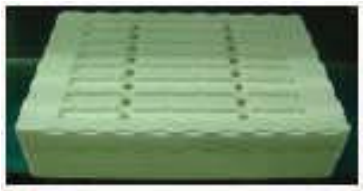
To put product into a ESD TRAY .(To put 60 products (6 pcs a layer, 11 layers a carton) into a carton witha vacant .



TSMT

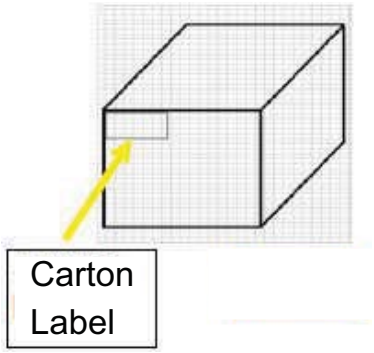






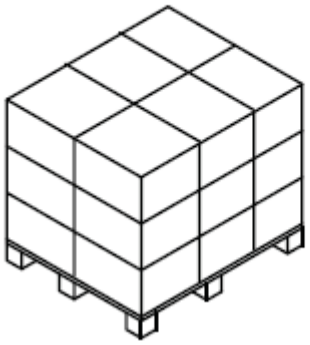
11layers a package

TO put product into a ESD TRAY.TO put 132 products (6pcs a layer, 2 packages a carton)



(To stack cartons was shown below FIG1.)

FIG1



(6 cartons per layer,
3 layers per pallet)

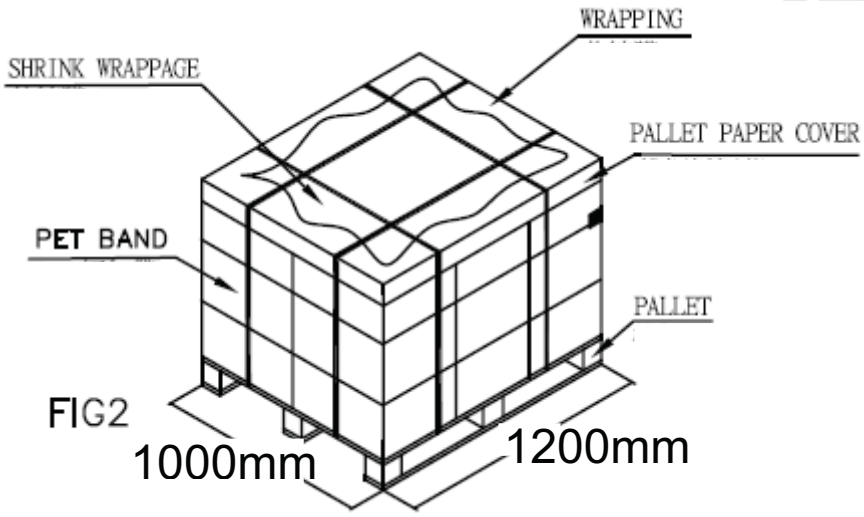
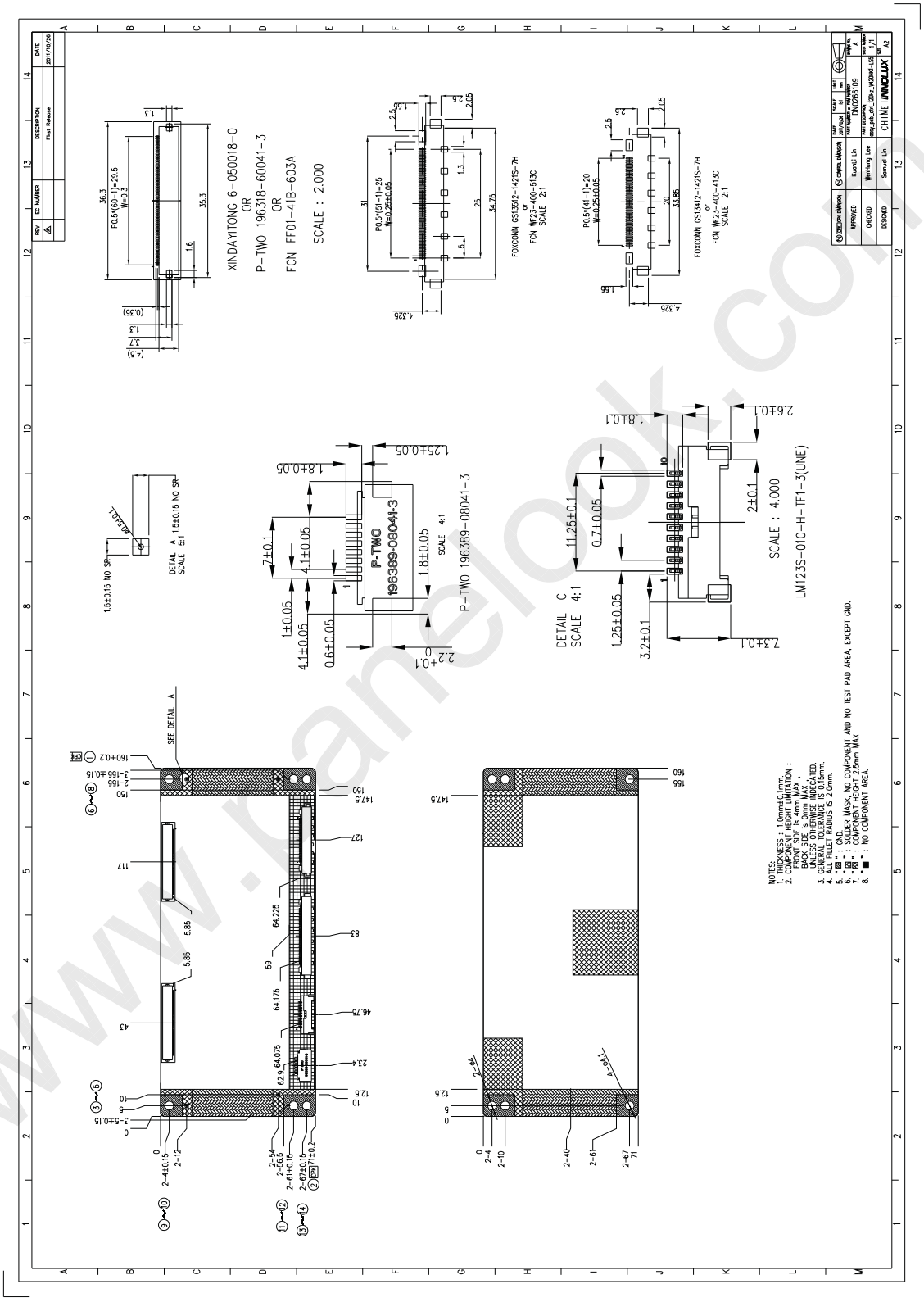


FIG2

10. MECHANICAL DRAWING



Appendix A

Local Dimming demo function

A.1 I2C address and write command

Device address: 0xe0

Register address: 0x65

Command data: 0x16 0x00 0x00 0x00 0x00 0x00: Local Dimming demo mode OFF (Note 1)

0x16 0x00 0x00 0x00 0x00 0x01 : Local Dimming demo mode ON (Demo in right half screen) (Note 2)

Preamble data: 0x26 0x38

I2C data:

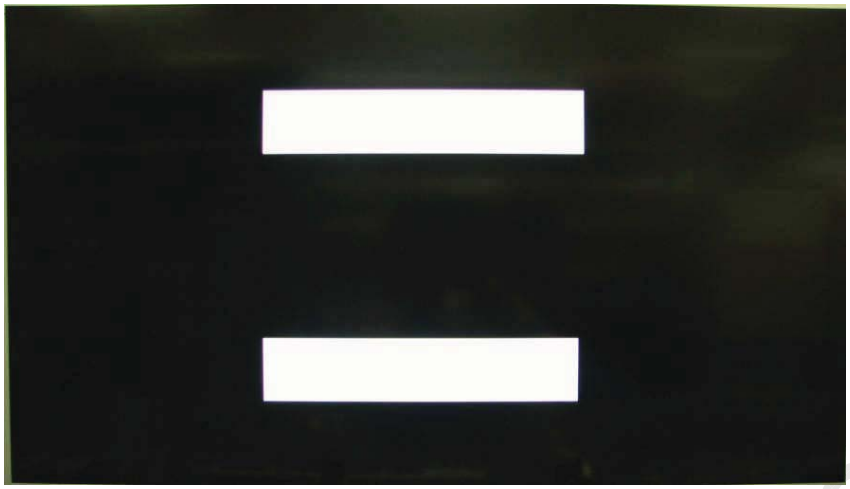
	Device Address		Preamble data		Preamble data	
START	11100000 (0xE0)	ACK	00100110 (0x26)	ACK	00111000 (0x38)	ACK

	Register Address		Command Data		Command Data	
	01100101 (0x65)	ACK	00010110 (0x16)	ACK	00000000 (0x00)	ACK

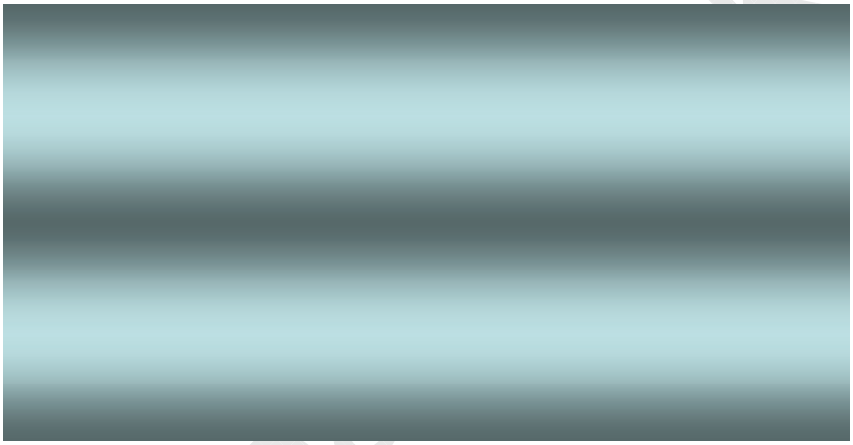
	Command Data		Command Data		Command Data	
	00000000 (0x00)	ACK	00000000 (0x00)	ACK	00000000 (0x00)	ACK

	Command Data	
	00000001 (0x01)	STOP

Note 1: Local Dimming demo OFF



Note 2: Local Dimming demo ON



A.2 I2C timing

Symbol	Parameter	Min.	Max.	Unit
t_{SU-STA}	Start setup time	250	-	ns
t_{HD-STA}	Start hold time	250	-	ns
t_{SU-DAT}	Data setup time	80	-	ns
t_{HD-DAT}	Data hold time	0	-	ns
t_{SU-STO}	Stop setup time	250	-	ns
t_{BUF}	Time between Stop condition and next Start condition	500	-	ns